## 30.4 A 2Mb/s Wideband Pulse Transceiver with Direct-Coupled Interface for Human Body Communications

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Wearable or implantable biomedical devices [1] can be used for health management using body area connectivity. There are two approaches to implementing on-body networks [2]. One using the human body as a transmission medium and the other using external medium for data transmission. The later category is also composed of wireline and RF technologies. Wireline technology can provide high data rates but needs long copper wires which is inconvenient for human body applications. The RF personal area connection using Bluetooth or ZigBee has low data rate, high power consumption, and vulnerability to interference problems.

Recently proposed [3]-[5] human body communication schemes, use the human body itself as the data transmission medium. Historically, near-field electrostatic coupling using a low frequency signal was first to be developed, but, it is dependent on the conditions of the surrounding environment such as the earth ground for the return path, and it has limited data rate due to the narrow bandwidth of 400kHz [3]. Another scheme employing an electromagnetic wave of 10MHz [4] also suffers from the bandwidth limitation of conventional FM and FSK. Alternatively, a recently developed transceiver using an electroopic sensor to achieve data rates of 10Mb/s [5] requires a special off-chip sensor, resulting in high cost, high power consumption, and low integration level. Moreover, it must have both signal and ground electrodes.

This paper presents a new human body communication method, a wideband signaling (WBS) transceiver with a direct-coupled interface (DCI) to achieve lower power consumption and higher data rate. In addition, it uses only a single electrode for data transmission, in contrast to other methods which require the off-chip sensor to detect the electric field and the earth ground path. The proposed human body communications using the DCI in the body area environment is illustrated in Fig. 30.4.1.

For the optimization of the WBS transceiver circuit, the characteristics of the human body channel are investigated with the DCI. As shown in Fig. 30.4.2, a battery-powered crystal-based transmitter is connected on the forearm with a single Ag/AgCl electrode. An electrode as a receiver is connected to a digital oscilloscope and its ground is floated to isolate it from the signal ground of the transmitter. In this setup, the transmitter transfers the electromagnetic pulse only through the forearm to the oscilloscope without the earth ground path. For the step input, the output is a pulse signal with a width of about 8ns, corresponding to a bandwidth of 125MHz. In the frequency-domain, the human body behaves as a BPF with a bandwidth of about 100MHz and approximately 5dB attenuation. The power attenuation between both forearms is approximately 10-15dB. A lumped electrical model for the DCI is obtained by modification of a previous simplified electrical model ($R_{ext}$, $C_{int}$, and $R_{int}$) for biological tissues [6]. The capacitance of $C_{air}$, a capacitor model associated with the electrostatic coupling via air as the return path, is very small due to the feeble electric field. According to this investigation, the suitable frequency for the WBS in the human body channel is determined to exist in the range of 10kHz to 100MHz, which is named the *"Bodywire channel"*.

The proposed transceiver architecture adopts the WBS technique exploiting the *Bodywire* channel. Figure 30.4.3 shows the block diagram of the transceiver that comprises a NRZ data transmitter and a CDR-based WBS receiver. The receiver AFE amplifies, triggers, and level shifts the received signal. A wide bandwidth preamplifier provides sufficient amplification to a pulse signal although it is corrupted by the channel. Next, the Schmitt trigger generates positive and negative states, and then the signal is shifted up to ground level for the next CDR.

Since the transceiver operates at relatively low data rates, distinct from gigabit serial links [7], bandwidth-limited effects and clock frequency offset between a transmitter and a receiver are tolerable in the WBS transceiver. In order to reduce the power consumption, a low supply voltage can be used [1]. However, if the supply voltage level, 1V in this design, is below the sum of the threshold voltage of NMOS and PMOS, an analog circuit like the CDR circuit faces performance degradation. To avoid this, the transceiver incorporates an all-digital sampling CDR architecture based on a DCO. To further reduce power consumption and complexity, a quadratic sampling technique is adopted. The structure of the quadratic sampling CDR circuit is similar to the all-digital PLL as illustrated in Fig. 30.4.4. The quadratic sampling phase detector (QSPD) samples the incoming data at every rising edge of the clock and detects the transition of the data. It provides quadratic gains over a bit interval window. With the QSPD, the number of sampling clock signals can be reduced by a factor of two, resulting in low power consumption and small area. The DCO based on a switched NMOS capacitor array is digitally controlled by FT[3:0], which is generated by averaging and low-pass filtering the sampled values through the lock-state controller. Its tuning range is 800kHz with the tuning gain of 50kHz/bit. The single delay stage of the DCO has a fully differential structure with a PMOS differential input pair in order to achieve lower flicker noise.

A test DCI is implemented with a PCB including a single Ag/AgCl electrode powered by an alkaline battery. Figure 30.4.5 shows the measured eye diagrams of input data, recovered clock and data for 2Mb/s $2^7$-1 PRBS, exhibiting a recovered clock jitter of 1.4ns rms. The WBS transceiver chip shown in Fig. 30.4.6 is fabricated using a 0.25μm standard CMOS technology and its core area is 0.85mm$^2$. Its power consumption is less than 0.2mW using a single 1V supply. Figure 30.4.7 summarizes the performance of the fabricated WBS transceiver and the comparison with previous works.

*References:*

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[2] Roy L. Ashok, et al., "Next-Generation Wearable Networks," *IEEE Computer Mag.*, pp.31-39, Nov., 2003.

[3] T. G. Zimmerman, "Personal Area Networks (PAN): Near-Field Intra-Body Communication," M.S. thesis, MIT, Sept., 1995.

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[5] M. Shinagawa, et al., "A Near-Field-Sensing Transceiver for Intrabody Communication Based on the Electrooptic Effect," *IEEE Trans. Instrum. Meas.*, vol. 53, pp. 1533-1538, Dec., 2004.

[6] L. C. Ward, et al., "Reliability of Multiple Frequency Bioelectrical Impedance Analysis: An Intermachine Comparison," *Amer. J. Hum. Biol.*, 9:63-72, 1997.

[7] S.-J. Song, et al., "A 4-Gb/s CMOS Clock and Data Recovery Circuit Using 1/8-Rate Clock Technique," *IEEE J. Solid State Circuits*, vol. 38, no. 7, pp. 1213-1219, July, 2003.

 

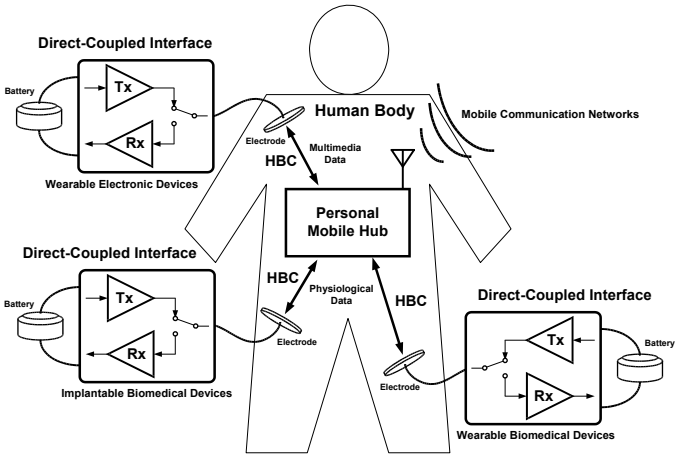


Figure 30.4.1: Conceptual diagram of human body communications in the body area environment.

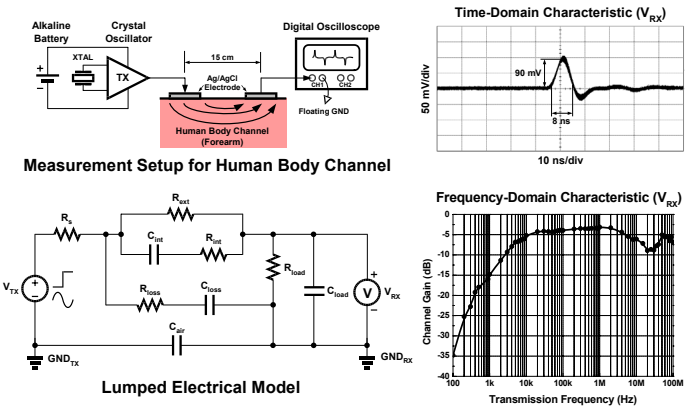


Figure 30.4.2: Characteristics of the human body channel, *Bodywire*.

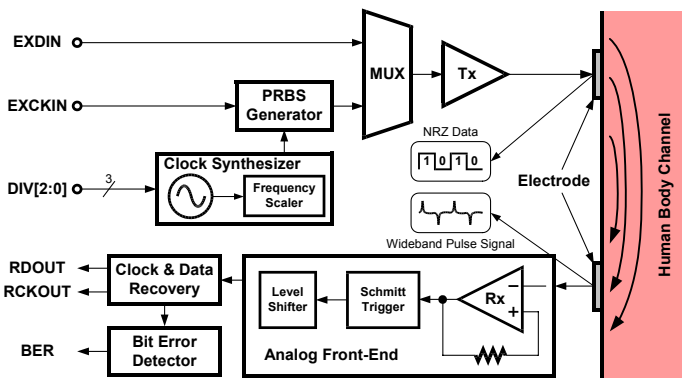


Figure 30.4.3: Block diagram of the proposed WBS transceiver.

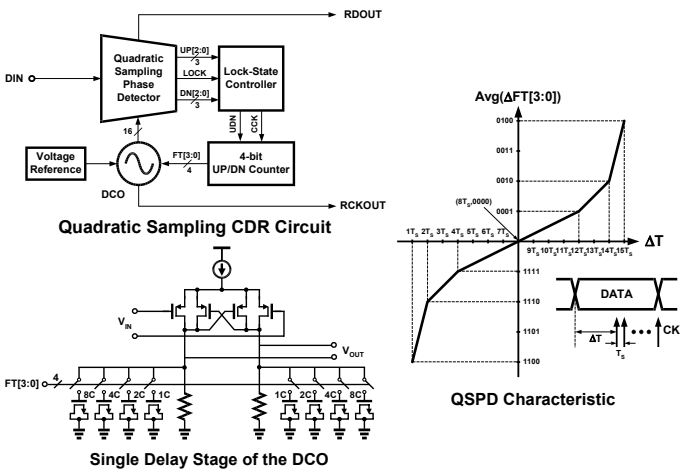


Figure 30.4.4: Quadratic sampling CDR circuit based on DCO.

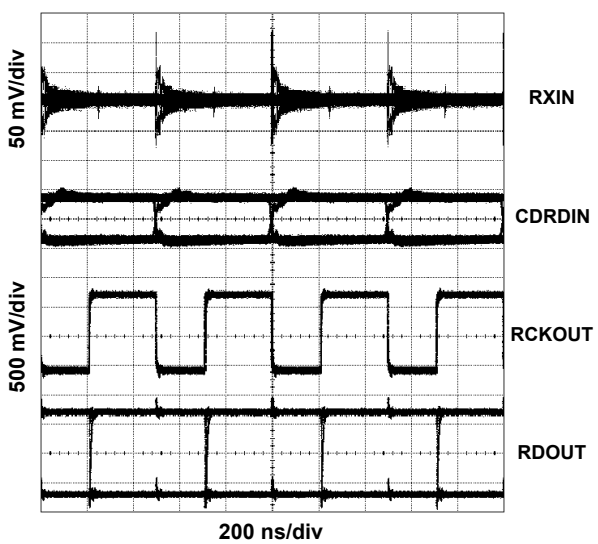


Figure 30.4.5: Measured eye diagrams of input data, recovered clock and data.

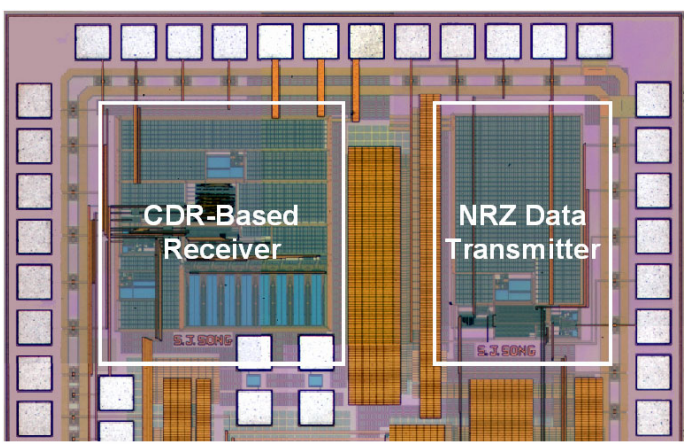


Figure 30.4.6: Micrograph of the test chip.

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| | [3] | [4] | [5] | This Work |
|---|---|---|---|---|
| Communication Method | Narrowband Modulation | Narrowband Modulation | Electrooptic Conversion | Wideband Signaling |
| Electrode | Signal, Ground | Signal, Ground | Signal, Ground | Signal |
| TX Architecture | LC Tank Oscillation | FM/FSK Modulation | Signal Boosting | NRZ Data Driving |
| RX Architecture | Current Integration | FM/FSK Demodulation | Threshold Comparison | Clock and Data Recovery |
| Modulation | OOK/DSSS | FM/FSK | No | No |
| Integration Level | Moderate | Moderate | Low | High |
| Data Rate | 2.4 kb/s | 9.6 kb/s | 10 Mb/s | 2 Mb/s |
| Supply Voltage | 9 V | 3 V | 5 V | 1 V |
| Power Consumption | 400 mW [1)] | Not reported | 650 mW | 0.2 mW [2)] |
| Bit Error Rate | Not reported | Not reported | $4.7 \times 10^{-8}$ | $< 10^{-7}$ |

1) Estimated by reference [3]
2) Excluding the AFE

**Figure 30.4.7: Performance summary and comparison with previous works.**

 